



Simulation Acceleration at DiBcom

DiBcom Background

DiBcom specializes in mobile television. We are a fabless semiconductor company that designs high-performance chipsets for wireless TV applications in the automotive, PC peripheral and handheld device markets. Our expertise is in mobile Digital Terrestrial Television (DTT) reception and we have developed patented algorithms and architectures for fast and accurate channel estimation and high Doppler compensation. Our goal is to provide high quality mobile TV service to those traveling by car or train, at speed up to 150 miles per hour, over hundreds of miles. Our chipsets are compliant with the current worldwide Digital Video Broadcast standards DVB-T and DVB-H.

DiBcom's Verification Challenge

Not including RAM, our chip is roughly two million gates. It processes real time video images, however, which is a real challenge for commercial simulation tools. Our simulation runtimes were becoming exceedingly long.

We began investigating hardware-based verification to decrease simulation time. Our team had some initial hesitation to go with an FPGA-based platform due to the longer compile time, but FPGA-based platforms have a significant simulation speed advantage over processor-based platforms. Also, we did not want to rewrite the RTL for the purpose of FPGA mapping, as is usually necessary when partitioning into multiple FPGAs.

DiBcom's Verification Flow

Our design flow includes both C++ level and register transfer level (RTL) models, so we use co-simulation of RTL blocks with C++ blocks. We also use HDL co-simulation where the core is being accelerated in FPGA hardware while the chip interfaces and analog cells are simulated using Cadence's mixed VHDL/Verilog NCSIM.

DiBcom Selects ZeBu

We chose EVE's ZeBu for our hardware assisted verification platform. The factors that most influenced us were ZeBu's ease-of-use, and its automatic partitioning across multiple FPGAs which facilitates the mapping effort during repeated design iterations. ZeBu's HDL/C++ co-simulation mode also enabled us to seamlessly plug it into our simulation environment. Finally, ZeBu had the performance to run real world video signals through our chip, which was an absolute requirement.

ZeBu Results

We use ZeBu for simulation acceleration primarily during two phases of our verification flow – block-level test and chip-level regression. It also enables us, however, to start configuring and fine-tuning the chip before committing to silicon, which can be seen as early software development.

We use ZeBu both day and night when processing real time video signals. The biggest advantage ZeBu gives us is the ability to detect bugs deeply embedded in the design that can be detected only by long simulation runs and processing real world signals.

With ZeBu in C++ cycle-based co-simulation mode we have been able to achieve a 300X speedup over our past HDL simulation times, thus reaching up to 1/1000 of the real-time speed.

One particularly interesting bug we found with ZeBu was when we ran simulation for many hours and detected a problem with a complex state machine going into a wrong state under very specific conditions. The extra test that showed the bug would not have been run without ZeBu.



ZeBu Case Study

What DiBcom Likes Most About ZeBu

"We like ZeBu's speed and ease of use – particularly with respect to automatic partitioning. Running in C++ cycle-based co-simulation we have seen a speedup of 300X over HDL simulation. David Brochart, Digital Design Engineer, DiBcom

The Bottom Line:

"Using ZeBu we are able to simulate our entire chip using real world video signals."

For further information about DiBcom, email info@dibcom.com or visit www.dibcom.com